REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, the applicants respectfully submit that the pending claims are not anticipated under 35 U.S.C. § 102 and are not rendered obvious under 35 U.S.C. § 103. Accordingly, it is believed that this application is in condition for allowance. **If, however, the Examiner believes that there are any unresolved issues, or believes that some or all of the claims are not in condition for allowance, the applicants respectfully request that the Examiner contact the undersigned to schedule a telephone Examiner Interview before any further actions on the merits.**

The applicants will now address each of the issues raised in the outstanding Office Action.

Objections

The amendment filed on August 4, 2005 was objected to under 35 U.S.C. § 132(a) as introducing new subject matter -- namely that "charges of said solid-state imaging element are read separately, one at a time." Since this recitation has been deleted from the claims, this objection should be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 1-6, 30-33, 35 and 36 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,786,852 ("the Suzuki patent"). The applicants

respectfully request that the Examiner reconsider and withdraw this ground of rejection in view of the following.

First, since claims 2, 4-6, 30-33, 35 and 36 have been canceled, this ground of rejection is rendered moot with respect to these claims.

According to the present invention, as described on page 16, line 23 to page 17, line 15, the saturated level of the horizontal transfer path (SatH) is not equal to, but instead larger than, the overflow level (OFL) of the CCD 105. Therefore, as shown in Fig. 6, taking k ($\neq$ 1, in this case 1.4) in equation (1) into account (k = SatH/OFL), the substrate bias voltage (V_{SUB}) in adding n pixels can be made lower (or the overflow level (OFL) can be made higher) than that in Fig. 5. The substrate bias voltage V_{SUB}, in adding n pixels, is set to such a value as makes the overflow level (OFL) become OFLr x k/n. For example, in adding two pixels, the substrate bias voltage (V_{SUB}) has only to be set to such a value (10.8V) as makes the overflow level (OFL) become 518(= 740 x 1.4/2) mV. As another example, in adding four pixels, the substrate bias voltage (V_{SUB}) has only to be set to such a value (13.5V) as makes the overflow level (OFL) become 259 (= 740 x 1.4/4) mV.

Taking into account the relationship (coefficient k in equation (1)) between the overflow level (OFL) of the charge accumulating portion and the saturated level of the horizontal transfer path (SatH), the set value of the substrate bias voltage V_{SUB} is determined, making the overflow level (OFL) of the charge accumulating portion higher than that in Fig. 5. This lowers the substrate bias voltage (V_{SUB}). Decreasing the variable range of the

substrate bias voltage (V_{SUB}) not only facilitates the design of the power supply, but also prevents, for example, a great change in the substrate bias voltage (V_{SUB}) from causing a disadvantage, such as a decrease in the effective sensitivity or a change in the spectral characteristic.

Although the Examiner states that the Suzuki patent teaches a saturated level of a horizontal transfer path included in the solid-state imaging element, citing column 13, line 54 to column 14, line 10 (See Paper No. 20051031, page 5.), the Suzuki patent does not control the substrate bias voltage (or the overflow level of the charge accumulating portion) such that the substrate bias voltage in the n-addition driving mode is a value obtained by multiplying (k/n) with the substrate bias voltage in the normal driving mode, k being SatH/OFL, SatH being a saturated level of the horizontal transfer path, and OFL being an overflow level of the charge accumulating portion. The Suzuki patent merely teaches that the saturation capacity of an interline solid-state image sensing device depends mainly on four factors including (3) the saturation value of a horizontal transfer part of the CDD (HCDD) (This value is determined by the maximum transfer capacity of the HCDD.) on column 14, lines 7-9.

The Suzuki patent controls the bias level and/or timing of a vertical transfer pulse depending on the operation mode selected via the mode switching device. (See, e.g., the Abstract.) The Suzuki patent aims to achieve a high sensitivity and a greater dynamic range. (See, e.g., column, 2, line 15.) In the field mode of the Suzuki patent, signals of all pixels are acquired

into the vertical transfer part, signals of two pixels adjacent in the vertical direction are added together, and the resultant signals are transmitted to in the vertical transfer part. (See e.g., column 1, lines 31-35.) Therefore, the Suzuki patent does not teach a control of the saturation level of the horizontal transfer path, even though the saturation level of the vertical transfer path may be controlled. Stated another way, the signal charges are added by the horizontal transfer path in the present invention (See, e.g., page 2, lines 2-12.) but are added by the vertical transfer path in the Suzuki patent.

Independent claim 1, as amended, is not anticipated by the Suzuki patent for at least the foregoing reasons. Since claim 3 depends from claim 1, it is similarly not anticipated.

Claims 11 and 12 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,661,451 ("the Kijima patent"). Since these claims have been canceled, this ground of rejection is rendered moot.

Rejections under 35 U.S.C. § 103

Claim 34 stands rejected under 35 U.S.C. § 103(a) as being anticipated by the Suzuki patent in view of the Kijima patent. Since this claim has been canceled, this ground of rejection is rendered moot.

Conclusion

In view of the foregoing amendments and remarks, the applicants respectfully submit that the pending claims are in condition for allowance. Accordingly, the applicants request that the Examiner pass this application to issue.

Respectfully submitted,

March 17, 2006

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CERTIFICATE OF MAILING under 37 C.F.R. 1.8(a)

I hereby certify that this correspondence is being deposited on **March 17, 2006** with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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